EXHIBIT 6

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

KAIST IP US LLC, Plaintiff and Counterclaim-Defendant, v. SAMSUNG ELECTRONICS CO., LTD.; SAMSUNG ELECTRONICS AMERICA, INC.; SAMSUNG SEMICONDUCTOR, INC.; SAMSUNG AUSTIN SEMICONDUCTOR, LLC; GLOBALFOUNDRIES, INC.; GLOBALFOUNDRIES U.S. INC.; and QUALCOMM INC., Defendants and Counterclaim-Plaintiffs.	Case No.: 2:16-cv-01314-JRG-RSP Honorable Rodney Gilstrap

REBUTTAL EXPERT REPORT OF KELIN J. KUHN, PH.D.

my Opening Report. Evidence of this commercial success includes the following:

- The significant performance, energy, and cost advantages conferred by the infringing bulk FinFET design as referenced in ¶¶ 419 to 473 of my Opening Report.
- The significant performance, energy and cost advantages conferred by the infringing bulk FinFET design as referenced in the Report of Mr. David Witt.
- The advertising by Samsung, Globalfoundries, and Qualcomm focused on the infringing bulk FinFET design, and the performance, energy and cost advantages of the 14 nm process technology reference in my Opening Report, the Witt Report, and the Weinstein Report.

733. I believe that the success of the ’055 Patent transistor design, and in particular the simultaneous performance, power and cost benefits were unexpected. There are at least two reasons for this. First, at the time of the ’055 Patent, the 40-year trend of semiconductor design was to make features planar. Processes universally included steps (such as polish) explicitly designed to keep features flat. The idea that a non-planar technology could yield sufficiently well to be cost-effective strongly opposed the collective insight of years of process development. Second, as process technologies shrunk to 20 nm it was unclear whether it would be possible to continue to obtain improvements in all three factors together. As the Witt Report and my Opening Report ¶¶ 348-60 discussed, 20 nm planar was an extremely disappointing node. In contrast, 14 nm was able to simultaneously achieve significant improvements in speed and power efficiency.

734. As noted previously, it is proper to attribute the speed, energy, and cost efficiency benefits of transitioning from 28 nm (or 20 nm) to 14 nm FinFET designs, as having provided

two benefits: the benefit of node shrinkage and the intrinsic benefit of the FinFET transistor design. I believe that these benefits are the result of the FinFET design described in the patent. It is this design that allowed for the node shrinkage below 20 nm (the practical scaling limit for planar devices at that time) and also reflects the intrinsic benefit of the FinFET design.

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737. Moreover, the adoption of the ’055 Patent design is not an isolated event by the Defendants. There has been industry embrace of the patented design. This is established based on the following. There are three major players in the commercial foundry space for ARM-based processors: Samsung, Globalfoundries, and TSMC. As noted in my Opening Report, Samsung and Globalfoundries both infringe the ’055 Patent. As noted in my Opening Report ¶¶ 318-414, Samsung’s following 10 nm process technology also infringes the ’055 Patent. Finally, as shown in **Appendix E**, based on recent technical information I have reviewed, TSMC’s 16 nm process technology also infringes the ’055 Patent.

738. During my time at Intel I was familiar with and had read Prof. Lee’s critical bulk FinFET research papers. I recognized these papers as critical and significant research in this space. Intel also recognized that bulk FinFET designs were fundamentally new. In 2011, Intel announced what it called “a fundamentally different technology for future microprocessor families: 3D transistors manufactured at 22 nm.” *See* KAIST-034991 (Joel Hruska, *Intel*

Announces New 22nm 3D Tri-Gate Transistors, HOTHARDWARE.COM (May 4, 2011), https://hothardware.com/news/intel-announces-new-22nm-3d-trigate-transistors). Intel's new chip, codenamed "Ivy Bridge," used a bulk FinFET device, which represented the world's first 3-D transistors for a high volume logic process. *Id.* This is the device that launched the modern FinFET revolution.

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1. Response to Subramanian Report

746. The Subramanian Report states that "there is no evidence that the '055 Patent added materially to bulk FinFET technology available at the time of the '055 Patent." Subramanian Report ¶ 1334.

747. [redacted]

B. Long Felt Need, Failure of Others and Skepticism

749. In my Declarations submitted with Patent Owners Preliminary Responses to the

this report (or any future report(s) I may prepare). Additionally, I anticipate making demonstrations utilizing some of the physical devices described in this report at trial.

XIII. CONCLUSION

850. Based on my analysis as set forth above, it is my opinion that claims 1-7, 9-17, and 19 of the '055 Patent are valid and enforceable.

Executed this 2nd day of March 2018 in Winthrop, Washington.

Kelin J. Kuhn

Kelin J. Kuhn, Ph.D.